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TRANSMITTAL OF APPEAL BRIEF (Large Entity)

Docket No.
EN9-98-072US2

In Re Application Of: **Enroth et al.**

Serial No.	Filing Date	Examiner	Group Art Unit
09/777,976	2/6/01	Chang, Rick Kiltae	3729

Invention: **WAVE SOLDER APPLICATION FOR BALL GRID ARRAY MODULES**

TO THE COMMISSIONER FOR PATENTS:

Transmitted herewith in triplicate is the Appeal Brief in this application, with respect to the Notice of Appeal filed on

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Docket No. EN9-98-072US2

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Enroth *et al.*

Group Art Unit: 3729

Filed: 2/6/01

Examiner: Chang, Rick Kiltae

Serial No.: 09/777,976

Title: **WAVE SOLDER APPLICATION FOR BALL GRID ARRAY MODULES**

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

BRIEF OF APPELLANT

This Appeal Brief, pursuant to the Notice of Appeal filed January 19, 2004, is an appeal from the rejection of the Examiner dated November 19, 2003.

REAL PARTY IN INTEREST

International Business Machines, Inc. is the real party in interest.

RELATED APPEALS AND INTERFERENCES

None.

STATUS OF CLAIMS

Claims 1, 5, 6, 8, 10, 12, 13, 15, 16, and 21-28 are currently pending. This Brief is in support of an appeal from the rejection of claims 1, 5, 6, 8, 10, 12, 13, 15, 16, and 21-28.

STATUS OF AMENDMENTS

There are no After-Final Amendment which have not been entered.

SUMMARY OF INVENTION

The present invention discloses a method for constructing a printed circuit board assembly. The printed circuit board is provided as comprising a top surface a top surface comprising a top pad, wherein the top pad is electrically connectable to a top component; a bottom surface; and a via extending through the circuit board from the top surface to the bottom surface, wherein the via is electrically connected to the top pad, and wherein the via includes an opening at the bottom surface. A plug is formed the via by inserting a volume of material into the via through the opening in the via. An end of the plug may be contacted with molten solder, wherein the end of the plug is at the bottom surface, and wherein the plug obstructs flow of the molten solder into the via. See FIGS. 5-7, and description thereof in Specification, page 7, line 6 - page 8, line 15.

The top component may be installed on the top surface, wherein a contact element of the top component is mechanically and electrically affixed to the top pad; the second component may be placed on the printed circuit board; and the bottom surface may be wave soldered, wherein the second component is mechanically and electrically affixed to the printed circuit board, and wherein the wave soldering provides the molten solder. See Specification, page 6, lines 1-12. Placement of the second component on the printed circuit board and the wave soldering may be performed after the plug is formed in the via. See Specification, page 8, lines 8-15.

The top component may be a surface mount device with a lead, wherein the contact element is the lead. See Specification, page 9, lines 8-11.

The second component may be a pin-in-hole component comprising a pin-component lead, wherein the pin-in-hole component is placed on the top surface, wherein the pin-component lead is directed from the top surface into a pin hole, and wherein the pin hole extends from the top surface to the bottom surface. See Specification, page 4, lines 2-4.

The via may be plugged while installing a bottom component onto the bottom surface, by a process comprising the steps of: screening solder paste, wherein the screening inserts solder paste into the opening in the via to form a solder mass within the via and onto a bottom pad located on the bottom surface to form a solder layer; placing the bottom component on the bottom surface, wherein the bottom component is in mechanical and electrical contact with the solder layer; and reflowing the solder mass and the solder layer, wherein the solder mass is redistributed within the via so as to form a plug in the via, and wherein the bottom component is mechanically and electrically affixed to the bottom surface. See Specification, page 7, line 19 - page 8, line 7; page 3, lines 14-20. A mask may be used to shield the bottom component from the effect of the wave soldering. See Specification, page 6, lines 9-12.

The installation of the top component may accomplished by a process comprising the steps of: screening solder paste onto the top pad to form a layer of solder; placing the top component on the top surface, wherein the contact element is in mechanical and electrical contact with the top pad; and reflowing the layer of solder, wherein the contact element is mechanically and electrically affixed to the top pad.. See Specification, page 6, lines 6-7.

The printed circuit board may further comprises a conductive lining on an interior wall of

the via such that the conductive lining is conductively coupled to the top pad. See Specification, page 6, lines 18-20.

The step of forming a plug comprises forming a solid plug, and wherein in the contacting step the solid plug obstructs flow of the molten solder into the via such as by contacting an end of the plug with molten solder, wherein the end of the plug is at the bottom surface of the printed surface board. See Specification, page 3, lines 4-6; FIG. 6.

ISSUES

1. Whether claims 1 and 21-23 are unpatentable under 35 U.S.C. §102(b) as allegedly being anticipated by Amago *et al.* (US 5,402,314).

2. Whether claims 5-6, 8, 10, and 24-28 are unpatentable under 35 U.S.C. §103(a) over Amago *et al.* (US 5,402,314) in view of Majd (US 5,155,904).

3. Whether claims 12-13 are unpatentable under 35 U.S.C. §103(a) over Sabotke *et al.* (US 5,737,834) in view of Nakaso *et al.* (US 5,638,598), and further in view of Lauffer *et al.* (US 5,867,898).

4. Whether claims 15-16 are unpatentable under 35 U.S.C. §103(a) over Sabotke *et al.* (US 5,737,834)/Nakaso *et al.* (US 5,638,598)/Lauffer *et al.* (US 5,867,898) as applied to claims 12-13 above, and further in view of Majd (US 5,155,904) and Thompson, Jr. (US 5,704,535).

GROUPING OF CLAIMS

The claims are grouped as shown in Table 1.

Table 1

Group	Issue	Claims	Do Claims of Group Stand or Fall Together?
1	1	1, 21-23	Yes
2	2	5	Yes
3	2	6	Yes
4	2	8, 10	Yes
5	2	24-28	Yes
6	3, 4	12-13, 15-16	Yes

The claims of Groups 2-6 do not stand and fall together with the claims of Group 1, because the claims of Groups 2-5 were rejected under 35 U.S.C. §103(a) whereas the claims of Group 1 was rejected under 35 U.S.C. §102(b).

The claims of Group 6 do not stand and fall together with the claims of Groups 1-5, because the claims of Group 6 were rejected over Sabotke in view of other references, whereas the with the claims of Groups 1-5 were not rejected over Sabotke.

The claim of Group 3 does not stand and fall together with the claims of Group 2, because the claim of Group 3 includes the following issue not present in the claim of Group 2: whether Amago in view of Majd teaches or suggests the feature: "wherein step (b) is followed by the steps of: placing a second component on the printed circuit board ..."

The claims of Group 4 do not stand and fall together with the claims of Groups 2-3, because the claims of Group 4 include the following issue not present in the claims of Groups 2-

3: whether the Examiner failed to establish a *prima facie* case of obviousness by failing to provide any argument for modifying Amago by the teaching of leaded components in Majd.

The claim of Group 5 does not stand and fall together with the claims of Groups 2-4, because the claim of Group 5 includes the following issue not present in the claims of Groups 2-4: whether Amago in view of Majd teaches or suggests the feature:

"plugging the via while installing a bottom component onto the bottom surface, by a process comprising the steps of:

screening solder paste, wherein the screening inserts solder paste into the opening in the via to form a solder mass within the via and onto a bottom pad located on the bottom surface to form a solder layer;

placing the bottom component on the bottom surface, wherein the bottom component is in mechanical and electrical contact with the solder layer; and

reflowing the solder mass and the solder layer, wherein the solder mass is redistributed within the via so as to form a plug in the via, and wherein the bottom component is mechanically and electrically affixed to the bottom surface"

ARGUMENT

Issue 1

CLAIMS 1 AND 21-23 ARE) ANTICIPATED BY AMAGO *ET AL.* (US 5,402,314).

The Examiner rejected claims 1 and 21-23 under 35 U.S.C. §102(b) as allegedly being anticipated by Amago *et al.* (US 5,402,314).

The Examiner argues: "Amago discloses in Fig. 12 with a solder resist 107 provided on

the bottom of the PCB to obstruct molten solder. 2 is a conductive lining and 5 is cured".

Claim 1

Appellants respectfully contend that Amago does not anticipate claim 1, because Amago does not teach each and every feature of claim 1.

As a first example of why Amago does not teach each and every feature of claim 1, Amago does not teach:

"(a) providing a printed circuit board comprising: a top surface comprising a top pad, wherein the top pad is electrically connectable to a top component; a bottom surface; and a via extending through the circuit board from the top surface to the bottom surface, wherein the via is electrically connected to the top pad, and wherein the via includes an opening at the bottom surface;

(b) forming a plug in the via by inserting a volume of material into the via through the opening in the via"

As a first step in the analysis of applying Amago to claim 1, Appellants will map the reference numerals and features in FIG. 12 of Amago to claim 1. The top surface of the printed circuit board (PCB) in FIG. 12 of Amago must be the surface to which the chip component 104 is attached, since claim 1 requires "a top surface comprising a top pad, wherein the top pad is electrically connectable to a top component". The bottom surface of the PCB in FIG. 12 of Amago must therefore be the surface to which the resist 107 is attached. The "opening" in the via 105 of FIG. 12 of Amago must be at the bottom surface of the PCB, since claim 1 recites: "wherein the via includes an opening at the bottom surface".

Given the preceding mapping of features of FIG. 12 of Amago to claim 1, Appellants contend that Amago does not teach a first feature of: "forming a plug in the via by inserting a volume of material into the via through the opening in the via". Appellants note that Amago is totally silent as to a method for achieving the structure shown in Fig. 12 of Amago. Therefore, Appellants further contend that the Examiner's allegation that Amago teaches forming the solder resist 107 in the through hole 105 by inserting a volume of material into the through hole 105 through the opening in the through hole 105 at the **bottom surface** of the PCB is pure speculation and is not disclosed anywhere in Amago. For example, the plug in FIG. 12 of Amago could have been formed by inserting, forcing, or flowing the solder resist 107 into the via 105 through an opening in the **top surface** of the via 105 until the resist reaches the bottom surface of the via 105 to have the configuration shown in FIG. 12 of Amago.

Appellants main point is that, since Amago does not disclose any process for forming the structure shown in FIG. 12, the only possibility for Amago to anticipate claim 1 is for the Examiner to demonstrate that the plug associated with the solder resist 107 is inherently formed by inserting the solder resist through the opening at the bottom surface of the PCB. However, Appellants have explained *supra* how the plug could be formed by inserting, forcing, or flowing the solder resist 107 into the via 105 through an opening in the top surface of the via 105. Therefore, the Examiner has not demonstrated the required inherency and, accordingly, Amago does not anticipate claim1.

As a second example of why Amago does not teach each and every feature of claim 1, Amago does not teach a second feature of: "contacting an end of the plug with molten solder,

wherein the end of the plug is at the bottom surface". Appellants maintain that in Fig. 12 of Amago, a top end of the plug (i.e., solder resist 107) is in the via 105 and **above** the bottom surface of the PCB, and a bottom end of the plug is **below** the bottom surface of the PCB. Appellants maintain that no end of the solder resist 107 is **at** the bottom surface of the printed circuit board, as required by claim 1. In addition, Amago discloses only the flow of molten solder at the top surface of the PCB into the hole 105 wherein the molten solder may contact only the top end of the plug (see Amago, col. 1, lines 48-51), and the top end of the plug is above the bottom surface of the PCB and not at the bottom surface of the PCB, as required by claim 1.

As a third example of why Amago does not teach each and every feature of claim 1, Amago does not teach a second feature of: "wherein the plug obstructs flow of the molten solder into the via". Amago discloses that molten solder that may enter the via 105 at the top of the via 105, resulting from soldering the chip component 104 to the land 106 (see Amago, col. 1, lines 48-51). Therefore, Appellants maintain that Amago does not disclose that the solder resist 107 obstructs flow of the molten solder into the via 105, but instead permits flow into the via 105 until being stopped by the plug of solder resist 107.

Based on the preceding arguments, Appellants respectfully maintain that Amago does not anticipate claim 1, and that claim 1 is in condition for allowance.

Claims 21-23

Since claims 21-23 depend from claim 1, which Appellants have argued *supra* to be not unpatentable under 35 U.S.C. §102(b), Appellants maintain that claims 21-23 are likewise not

unpatentable under 35 U.S.C. §102(b).

Issue 2

CLAIMS 5-6, 8, 10, AND 24-28 ARE NOT UNPATENTABLE UNDER 35 U.S.C. §103(a) OVER AMAGO *ET AL.* (US 5,402,314) IN VIEW OF MAJD (US 5,155,904).

The Examiner rejected claims 5-6, 8, 10, and 24-28 under 35 U.S.C. §103(a) as allegedly being unpatentable over Amago *et al.* (US 5,402,314) in view of Majd (US 5,155,904).

The Examiner argues: "Amago discloses placing and fixing top and bottom components (Fig. 2), lining an interior wall of the via (2), Fig. 9 shows 2 at the end of the bottom surface. Amago fails to disclose wave soldering and providing leaded components. Majd discloses wave soldering (Fig. 1) and providing leaded and PIH components (44, 46, 53, 54 and 55). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Amago by wave soldering and providing leaded and PIH components, as taught by Majd, for the purpose of increasing production by mass soldering IC components."

Claim 5

A first reason why claim 5 is not unpatentable over Amago in view of Majd is that Amago in view of Majd does not teach or suggest "contacting an end of the plug with molten solder, wherein the end of the plug is at the bottom surface, and wherein the plug obstructs flow of the molten solder into the via". FIG. 2 of Amago does not teach or suggest that an end of the plug 5 is at the bottom surface of the via 2. FIG. 9 of Amago does not teach or suggest that an end of the plug in the via is contacted by molten solder such that the end of the plug is at the bottom surface of the printed circuit board. FIG. 1 of Majd certainly does not disclose contacting

an end of a plug in a via with molten solder.

A second reason why claim 5 is not unpatentable over Amago in view of Majd is that the Examiner has not provided an argument for combining FIGS. 2 and 9 of Amago.

A third reason why claim 5 is not unpatentable over Amago in view of Majd is that the Examiner's reason for modifying Amago by the teaching of wave soldering in step 27 of Fig. 1 of Majd is not persuasive, because there is no indication in Amago of any need for increasing mass production; adding wave soldering to Amago would unnecessarily add unnecessary expense and would not further the objects of Amago's invention as disclosed in Amago, col. 1, line 61 - col. 2, line 4. Furthermore, the Examiner's argument lacks a supporting analysis and is thus additionally not persuasive.

Claim 6

A first reason why claim 6 is not unpatentable over Amago in view of Majd is that neither Amago nor Majd teach or suggests forming the plug **before** placing the second component on the printed circuit board, and the Examiner has not made any argument in this regard. See the following language in claim 6: "wherein step (b) is **followed** by the steps of: placing a second component on the printed circuit board ..." (emphasis added).

A second reason why claim 6 is not unpatentable over Amago in view of Majd is that Amago in view of Majd does not teach or suggest "contacting an end of the plug with molten solder, wherein the end of the plug is at the bottom surface, and wherein the plug obstructs flow of the molten solder into the via". FIG. 2 of Amago does not teach or suggest that an end of the plug 5 is at the bottom surface of the via 2. FIG. 9 of Amago does not teach or suggest that an

end of the plug in the via is contacted by molten solder such that the end of the plug is at the bottom surface of the printed circuit board. FIG. 1 of Majd certainly does not disclose contacting an end of a plug in a via with molten solder.

A third reason why claim 6 is not unpatentable over Amago in view of Majd is that the Examiner has not provided an argument for combining FIGS. 2 and 9 of Amago.

A fourth reason why claim 6 is not unpatentable over Amago in view of Majd is that the Examiner's reason for modifying Amago by the teaching of wave soldering in step 27 of Fig. 1 of Majd is not persuasive, because there is no indication in Amago of any need for increasing mass production; adding wave soldering to Amago would unnecessarily add unnecessary expense and would not further the objects of Amago's invention as disclosed in Amago, col. 1, line 61 - col. 2, line 4. Furthermore, the Examiner's argument lacks a supporting analysis and is thus additionally not persuasive.

Claim 8

Since claim 8 depends from claim 5, which Appellants have argued *supra* to be not unpatentable under 35 U.S.C. §103(a), Appellants maintain that claim 8 is likewise not unpatentable under 35 U.S.C. §103(a).

Another reason why claim 8 is not unpatentable over Amago in view of Majd is that the Examiner has not provided any argument for modifying Amago by the teaching of leaded components in Majd. By not providing any argument, the Examiner has failed to establish a *prima facie* case of obviousness in relation to claim 8.

Claim 10

Since claim 10 depends from claim 5, which Appellants have argued *supra* to be not unpatentable under 35 U.S.C. §103(a), Appellants maintain that claim 10 is likewise not unpatentable under 35 U.S.C. §103(a).

Another reason why claim10 is not unpatentable over Amago in view of Majd is that the Examiner has not provided any argument for modifying Amago by the teaching of leaded components in Majd. By not providing any argument, the Examiner has failed to establish a *prima facie* case of obviousness in relation to claim 10.

Claims 24-28

Claim 12 is not unpatentable over Amago in view of Majd, since claim 12 was not rejected over Amago in view of Majd. Since claims 24-28 depend from claim 12, claims 24-28 are likewise not unpatentable over Amago in view of Majd.

Moreover, none of the Examiner's arguments relating to the rejection of claims 5-6, 8, 10, and 24-28 over Amago in view of Majd relate to the following feature of claim 12 which is also a feature of claims 24-28:

"plugging the via while installing a bottom component onto the bottom surface, by a process comprising the steps of:

screening solder paste, wherein the screening inserts solder paste into the opening in the via to form a solder mass within the via and onto a bottom pad located on the bottom surface to form a solder layer;

placing the bottom component on the bottom surface, wherein the bottom

component is in mechanical and electrical contact with the solder layer; and

reflowing the solder mass and the solder layer, wherein the solder mass is redistributed within the via so as to form a plug in the via, and wherein the bottom component is mechanically and electrically affixed to the bottom surface."

By not providing any argument with respect to the preceding feature of claims 24-28, the Examiner has failed to establish a *prima facie* case of obviousness in relation to claims 24-28.

Issue 3

CLAIMS 12-13 ARE NOT UNPATENTABLE UNDER 35 U.S.C. §103(a) OVER SABOTKE *ET AL.* (US 5,737,834) IN VIEW OF NAKASO *ET AL.* (US 5,638,598), AND FURTHER IN VIEW OF LAUFFER *ET AL.* (US 5,867,898).

The Examiner rejected claims 12-13 under 35 U.S.C. §103(a) as allegedly being unpatentable over Sabotke *et al.* (US 5,737,834) in view of Nakaso *et al.* (US 5,638,598), and further in view of Lauffer *et al.* (US 5,867,898).

The Examiner alleges: "Sabotke discloses in Fig. 1 steps of applying solder paste, reflow soldering components, and fixing a second component onto the PCB. In light of the claimed invention, Sabotke's components mounted on the top surface will be the bottom components mounted in the claimed invention, and vice versa. Sabotke fails to disclose providing a PCB having a soldered via electrically communicating between layers as well as top to bottom layers and screen printing solder. Nakaso discloses in Fig. 3 a solder plug in a via formed in a PCB. Lauffer discloses in claim 8 screening the solder paste. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Sabotke by providing a PCB having a soldered via electrically communicating between layers as well as top to bottom

layers and screen printing solder, as taught by Nakaso and Lauffer, for the purpose of allowing forming densely formed contacts to electrically communicate between layers and top and bottom surfaces, as well as increase production by mass soldering a plurality of vias and pads."

Claims 12-13

Applicant contends that Lauffer cannot be used as prior art in rejecting claims 12-13, because "[e]ffective November 29, 1999, subject matter which was prior art under former 35 U.S.C. 103 via 35 U.S.C. 102(e) is now disqualified as prior art against the claimed invention if that subject matter and the claimed invention 'were, at the time the invention was made, owned by the same person or subject to assignment by the same person.'" MPEP 706.02(1)(1). First, the present patent was filed on February 6, 2001 which is after November 29, 1999. Second, the Lauffer patent is being considered by the Examiner as prior art under former 35 U.S.C. 103 via 35 U.S.C. 102(e), because the Lauffer patent issued on February 9, 1999 which is after the effective filing date of December 15, 1998 of the present patent application (based on priority of Serial Number 09/211,976, presently issued as U.S. Patent Number 5,867,898). Third, both the subject matter of Lauffer patent and the claimed invention of the present patent application were, at the time the invention was made, owned by International Business Machines Corporation or subject to assignment by International Business Machines Corporation. Accordingly, Applicant respectfully maintains that Lauffer cannot be used as a prior art reference.

In addition, Applicants contend that claims 12-13 are not unpatentable over Sabotke in view of Nakaso, and further in view of Lauffer because it is not obvious to modify Sabotke with

Lauffer's solder paste screening steps and with Nakaso's solder plug.

A first reason why the preceding combination of references is improper is that forming a via in Sabotke's PCB is irrelevant to Sabotke's invention. Sabotke invention relates only to the efficiency of installing components on the top and bottom surfaces of a PCB and is totally unconcerned with electrical communication between the components on the top surface and the components on the bottom surface. Applicants maintain that forming a via in Sabotke's PCB would in no way improve the invention that Sabotke discloses.

A second reason why the preceding combination of references is improper is that, even if it is obvious to form a via in Sabotke's PCB (which it isn't), it is not obvious to plug the via with a solder plug to satisfy the Examiner's stated reason of "allowing forming densely formed contacts to electrically communicate between layers and top and bottom surfaces". All that is required to satisfy the Examiner's stated reason is to have an electrically conductive material in the via continuously extending between the top and bottom surfaces of the PCB. It is irrelevant to the Examiner's stated reason for said electrically conductive material to function as a plug in the via. Indeed, having said electrically conductive material function as a plug will require more material and add unnecessary weight. In any event, Applicants maintain that it is not obvious for the said electrically conductive material to function as a plug in the via.

A third reason why the preceding combination of references is improper is that it is not obvious to form and plug the vias with a solder plug to satisfy the Examiner's stated reason of "increas[ing] production by mass soldering a plurality of vias and pads". Applicants contend that production by mass soldering will not be increased by forming plugs within the vias as compare to not forming plugs within the vias. Therefore, Applicants maintain that it is not obvious to

form a plug in the via.

Additionally, Applicants respectfully maintain that the Examiner's argument with respect to Nakaso is an improper modification of the secondary reference of Lauffer. The Examiner argues that the primary reference of Sabotke discloses "applying solder paste, reflow soldering components, and fixing a second component onto the PCB". The Examiner also argues that the secondary reference of Lauffer has modified the primary reference of Sabotke, by alleging that Lauffer teaches or suggests having a via in Sabotke's PCB and screening solder paste in said via. The Examiner additionally argues that the secondary reference of Nakaso has modified the secondary reference of Lauffer, by alleging that Nakaso teaches or suggests having the solder paste screened according to Lauffer form a sold plug in the via. Applicants maintain that it is improper to argue that a claim feature is taught or suggested by a secondary reference through modification of another secondary reference. If the Examiner could modify a secondary reference in the preceding manner, then the Examiner would be able to show the existence of any element or feature of any claim merely by chaining a sufficient number of secondary references together in the preceding manner. Accordingly, Applicants respectfully maintain that the rejection of claim 12 under 35 U.S.C. §103(a) is improper and should be withdrawn.

Issue 4

CLAIMS 15-16 ARE NOT UNPATENTABLE UNDER 35 U.S.C. §103(a) OVER SABOTKE *ET AL.* (US 5,737,834)/NAKASO *ET AL.* (US 5,638,598)/LAUFFER *ET AL.* (US 5,867,898) AS APPLIED TO CLAIMS 12-13 ABOVE, AND FURTHER IN VIEW OF MAJD (US 5,155,904) AND THOMPSON, JR. (US 5,704,535).

Since claims 15-16 depend from claim 13, which Appellants have argued *supra* to be not unpatentable under 35 U.S.C. §103(a), Appellants maintain that claims 15-16 are likewise not

unpatentable under 35 U.S.C. §103(a).

In addition, Applicant contends that Lauffer cannot be used as prior art in rejecting claims 15-16, because "[e]ffective November 29, 1999, subject matter which was prior art under former 35 U.S.C. 103 via 35 U.S.C. 102(e) is now disqualified as prior art against the claimed invention if that subject matter and the claimed invention 'were, at the time the invention was made, owned by the same person or subject to assignment by the same person.'" MPEP 706.02(1)(1). First, the present patent was filed on February 6, 2001 which is after November 29, 1999. Second, the Lauffer patent is being considered by the Examiner as prior art under former 35 U.S.C. 103 via 35 U.S.C. 102(e), because the Lauffer patent issued on February 9, 1999 which is after the effective filing date of December 15, 1998 of the present patent application (based on priority of Serial Number 09/211,976, presently issued as U.S. Patent Number 5,867,898). Third, both the subject matter of Lauffer patent and the claimed invention of the present patent application were, at the time the invention was made, owned by International Business Machines Corporation or subject to assignment by International Business Machines Corporation. Accordingly, Applicant respectfully maintains that Lauffer cannot be used as a prior art reference.

SUMMARY

In summary, Appellant respectfully requests reversal of the November 19, 2003 Office Action rejection of claims 1, 5, 6, 8, 10, 12, 13, 15, 16, and 21-28.

Respectfully submitted,

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Enroth *et al.* Group Art Unit: 3729

Filed: 2/6/01 Examiner: Chang, Rick Kiltae

Serial No.: 09/777,976

Title: **WAVE SOLDER APPLICATION FOR BALL GRID ARRAY MODULES**

Commissioner for Patents
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APPENDIX - CLAIMS ON APPEAL

1. A method for constructing a printed circuit board assembly, comprising the steps of:

(a) providing a printed circuit board comprising:

a top surface comprising a top pad, wherein the top pad is electrically connectable to a top component;

a bottom surface; and

a via extending through the circuit board from the top surface to the bottom surface, wherein the via is electrically connected to the top pad, and wherein the via includes an opening at the bottom surface;

(b) forming a plug in the via by inserting a volume of material into the via through the opening in the via; and

(c) contacting an end of the plug with molten solder, wherein the end of the plug is at the bottom surface, and wherein the plug obstructs flow of the molten solder into the via.

5. The method of claim 1, further comprising the steps of:

installing the top component on the top surface, wherein a contact element of the top component is mechanically and electrically affixed to the top pad;

placing a second component on the printed circuit board; and

wave soldering the bottom surface, wherein the second component is mechanically and electrically affixed to the printed circuit board, and wherein the wave soldering provides said molten solder.

6. The method of claim 1, wherein step (b) is preceded by the step of:

installing the top component on the top surface, wherein a contact element of the top component is mechanically and electrically affixed to the top pad;

and wherein step (b) is followed by the steps of:

placing a second component on the printed circuit board; and

wave soldering the bottom surface, wherein the second component is mechanically and electrically affixed to the printed circuit board, and wherein the wave soldering provides said molten solder.

8. The method of claim 5, wherein the top component is a surface mount device with a lead, wherein the contact element is the lead.

10. The method of claim 5, wherein the second component is a pin-in-hole component comprising a pin-component lead, wherein the pin-in-hole component is placed on the top

surface, wherein the pin-component lead is directed from the top surface into a pin hole, and wherein the pin hole extends from the top surface to the bottom surface.

12. A method for constructing a printed circuit board assembly, comprising the steps of:

(a) providing a printed circuit board comprising:

a top surface comprising a top pad, wherein the top pad is electrically connectable to a top component;

a bottom surface;

a middle layer between the top surface and the bottom surface comprising an electrical circuit pattern; and

a via extending through the circuit board from the top surface to the bottom surface, wherein the via is electrically connected to the top pad, wherein the via is electrically connected to the electrical circuit pattern, and wherein the via includes an opening at the bottom surface; and

(b) plugging the via while installing a bottom component onto the bottom surface, by a process comprising the steps of:

screening solder paste, wherein the screening inserts solder paste into the opening in the via to form a solder mass within the via and onto a bottom pad located on the bottom surface to form a solder layer;

placing the bottom component on the bottom surface, wherein the bottom component is in mechanical and electrical contact with the solder layer; and

reflowing the solder mass and the solder layer, wherein the solder mass is

redistributed within the via so as to form a plug in the via, and wherein the bottom component is mechanically and electrically affixed to the bottom surface; and

(c) installing the top component on the top surface, wherein a contact element of the top component is mechanically and electrically affixed to the top pad.

13. The method of claim 12, wherein the installation of the top component in step ©) is accomplished by a process comprising the steps of:

screening solder paste onto the top pad to form a layer of solder;

placing the top component on the top surface, wherein the contact element is in mechanical and electrical contact with the top pad; and

reflowing the layer of solder, wherein the contact element is mechanically and electrically affixed to the top pad.

15. (Original) The method of claim 13, further comprising the steps of:

(d) placing a pin-in-hole component on the top surface, wherein the pin-in-hole component comprises a pin-component lead, wherein the pin-component lead is directed from the top surface into a pin hole, and wherein the pin hole extends from the top surface to the bottom surface; and

(e) wave soldering the bottom surface, wherein the pin-in-hole component is mechanically and electrically affixed to the printed circuit board, and wherein a mask is used to shield the bottom component from the effect of wave soldering.

16. The method of claim 13, further comprising the steps of:

(d) placing a pin-in-hole component on the top surface, wherein the pin-in-hole component comprises a pin-component lead, wherein the pin-component lead is directed from the top surface into a pin hole, and wherein the pin hole extends from the top surface to the bottom surface; and

(e) wave soldering the bottom surface, wherein the pin-in-hole component is mechanically and electrically affixed to the printed circuit board, and wherein the bottom component is further affixed to the printed circuit board by the wave soldering.

21. The method of claim 1, wherein the printed circuit board further comprises a conductive lining on an interior wall of the via such that the conductive lining is conductively coupled to the top pad.

22. The method of claim 21, wherein the step of forming a plug comprises forming a solid plug, and wherein in the contacting step the solid plug obstructs flow of the molten solder into the via.

23. The method of claim 1, wherein the step of forming a plug comprises forming a solid plug, and wherein in the contacting step the solid plug obstructs flow of the molten solder into the via.

24. The method of claim 12, wherein the printed circuit board further comprises a conductive lining on an interior wall of the via such that the conductive lining is conductively coupled to the

top pad.

25. The method of claim 24, wherein the method further comprises the step of contacting an end of the plug with molten solder, wherein the end of the plug is at the bottom surface, and wherein the plug obstructs flow of the molten solder into the via.

26. The method of claim 25, further comprising:

placing a first component on the printed circuit board; and

wave soldering the bottom surface, wherein the first component is mechanically and electrically affixed to the printed circuit board, and wherein the wave soldering provides said molten solder.

27. The method of claim 12, wherein the method further comprises the step of contacting an end of the plug with molten solder, wherein the end of the plug is at the bottom surface, and wherein the plug obstructs flow of the molten solder into the via.

28. The method of claim 27, further comprising:

placing a first component on the printed circuit board; and

wave soldering the bottom surface, wherein the first component is mechanically and electrically affixed to the printed circuit board, and wherein the wave soldering provides said molten solder.